

Computer Architecture Group

Work Plans

1.1. Unified design of embedded system components

Level: B.Sc or M.Sc

Objective: The objective of this track is to develop embedded system components using a design methodology which allows the generation of both hardware and software from a unified description.

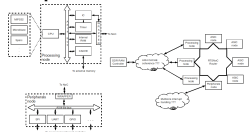
Activities:

- Study the state-of-art
- Define an application domain and components
- Implement and evaluate the components
- Publish the work

1.2. Implementation of a flexible MPSoC

Level: Any

Objective: The objective of this track is to implement a flexible Multiprocessor System-on-Chip (MPSoC) based on the AMBA AXI4 bus and on the RTSNoC network-on-chip. A base implementation of the SoC already exists, however, it currently supports a single core and a few IO peripherals. The final implementation may be similar to the figure bellow (some aspects are no yet defined):



[fig_soc.odg](#)

This work plan consists basically of technical activities, but it is possible (and recommended) to use the final MPSoC as a case study for research in the following topics:

- Intercore communication
- Network-on-Chips
- Cache coherence in multicore architectures
- And whatever

Activities:

- Study current implementation
- Define memory hierarchy and cache coherence protocols
- Define interrupt handling
- Implement and evaluate the MPSoC
- Publish your work